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10/767,065	01/29/2004	Toshiharu Furukawa	ROC920030268US1	5663

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/767,065	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (6,566,704).

Regarding claim 1, Choi et al. teach in figure 3F and related text a vertical transistor device structure formed on a substrate 200, the substrate 200 defining a substantially horizontal plane, the transistor device structure comprising:

a source region 40;

a drain region 50;

a gate electrode 20 disposed on the substrate, said gate electrode positioned vertically between said source region and drain region; and

a nanotube 100 including a first end physically and electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source region and said drain region, and

said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region between said source region and said drain region.

Choi et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes.

Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of a nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43). Choi et al. further teach in the embodiment of figure 4B connecting the plurality of semiconducting nanotubes 100 with a single drain region 50 and a single source region 40.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of unit cells of the transistor in Choi et al.'s device, such that a plurality of semiconducting nanotubes are present in the device, and to connect the plurality of semiconducting nanotubes with a single drain region and a single source region, in order to use the device in a practical application which requires a plurality of semiconducting nanotubes, such as a nano sized transistor, and in order to simplify the processing steps of making the device and to simplify the operation of the device, respectively.

Regarding claims 4-6 and 8, Choi et al. teach in figure 1 and related text an insulating layer 30 disposed between said drain and said gate electrode for

electrically isolating said drain from said gate electrode, an insulating layer 10 disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Choi et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced

by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Response to Arguments

1. Applicant argues that “the generalizations regarding the plural term "carbon nanotubes" made at column 3, lines 39-43 of Choi fail to support the Examiner's conclusion that the unit cell shown in Figures 1-3 of Choi can be modified to include more than one semiconducting nanotube”, because “The statement made in Choi at column 3, lines 39-43 is inconsistent with all other statements found in Choi that regard the first embodiment shown in Figures 1-3. At column 3, line 44, Choi refers to "a carbon nanotube 100", which uses the singular indefinite article "a". From column 3, line 45 to column 4, line 23, Choi consistently uses the term "the carbon nanotube" to characterize the unit cell shown in Figures 1-3. The term "nanotube" is singular, not plural. When describing the fabrication process in connection with Figure 3, Choi again refers to the growth of "a carbon nanotube". See col. 4, lines 20-22. Only a single nanotube 100 is visible in Figures 1-3 of Choi. When these statements considered as a whole, Choi is not suggesting that the embodiment shown in Figures 1-3 can be predictably modified to include a plurality of nanotubes”.

From column 3, line 45 to column 4, line 23, Choi consistently uses the term "the carbon nanotube", because Choi describes the process of making **a unit cell**, as shown in Figures 1-3. There is no reason for Choi to use the phrase "carbon nanotubes" when describing the process of making a unit cell which comprises only one carbon nanotube.

Choi explicitly states in column 3, lines 39-43, that "A vertical nano-sized transistor using carbon nanotubes according to the first embodiment of the present invention will now be explained. As shown in FIG. 1, a unit cell of a vertically aligned carbon nanotube transistor is constructed as follows". The ordinary meaning of the above phrase is that the description of the process of making the unit cell of figure 1, which comprises only one carbon nanotube, follows, whereas **the final structure** of the vertical nano-sized transistor comprises plurality of carbon nanotubes.

2. Applicant argues that "the Examiner's modification to add multiple nanotubes (100) to the embodiment of Figures 1-3 would lead a person having ordinary skill in the art to stack the gate electrode (20) and gate dielectric (30) above the plurality of nanotubes (100) as shown in Figures 4A and 4B", and "a person having ordinary skill in the art would not make the Examiner's proposed modification to the first embodiment disclose in Figures 1-3 of Choi".

The embodiment of figures 4A and 4B of Choi describes a structure which is separate and distinct from that of figure 3. If an artisan forms plurality of

carbon nanotubes in the embodiment of figure 3, as described in the embodiment of figure 4, as argued by applicant, then both structures will be identical. This is in contradiction to Choi's teaching who states that the embodiments of figures 3 and 4 are two separate and distinct structures.

The examiner stated that "Choi et al. further teach in the embodiment of figure 4B connecting the plurality of semiconducting nanotubes 100 with a single drain region 50 and a single source region 40", in order to teach an artisan that plurality of semiconducting nanotubes can be connected with a single drain region and a single source region.

3. Applicant argues that "The Examiner's rationale for modifying Choi is to "use a plurality of semiconducting nanotubes in Choi et al.'s device into order to use the device in a practical application which requires a plurality of semiconducting nanotubes" is circular".

It is well known in the art that a practical application uses plurality of carbon nanotubes and not a single carbon nanotube. The examiner respectfully requests applicant to provide evidence that practical industrial applications use only a single carbon nanotube.

4. Applicant argues that Figure 4B of Choi teaches "the drain lines (50) are arranged in parallel lines or stripes and the source lines (40) are likewise arranged in parallel lines or stripes that are oriented orthogonal to the stripes

representing the drain lines (50)", and thus "the Examiner's construction of Figure 4B of Choi is incorrect in that Figure 4B fails to disclose a plurality of nanotubes that are connected with a single source region and with a single drain region".

As stated above, an artisan will not form the device of figure 3 to have plurality of carbon nanotubes as described in the separate and distinct embodiment of figure 4. However, claim 1 recites that "a plurality of semiconducting nanotubes, each of said plurality of semiconducting nanotubes including a first end electrically coupled with said source region, a second end electrically coupled with said drain region". Claim 1 does not recite that each of said plurality of semiconducting nanotubes must including a first end which is physically connected with said source region, a second end which is physically with said drain region. Thus, even if an artisan makes the device of figure 3, as described in the embodiment of figure 3, which the examiner does not admit, then clearly the device of figure 4 includes "a plurality of semiconducting nanotubes, each of said plurality of semiconducting nanotubes including a first end **electrically** coupled with said source region, a second end **electrically** coupled with said drain region", as claimed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the

Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
5/3/2010

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